A Hexagon-Based Honeycomb Routing Architecture for FPGA

Kaichuang Shi, Hao Zhou, Lingli Wang*

State Key Laboratory of ASIC and System

Fudan University, Shanghai, China

{19112020058, zhouhao, llwang}@fudan.edu.cn

Outline

- Introduction
- Related work
- Honeycomb architecture
- Experimental result
- Conclusion & Future work

Outline

- Introduction
- Related work
- Honeycomb architecture
- Experimental result
- Conclusion & Future work

Introduction

LB: **L**ogic **B**lock
CB: **C**onnection **B**lock
SB: **S**witch **B**lock

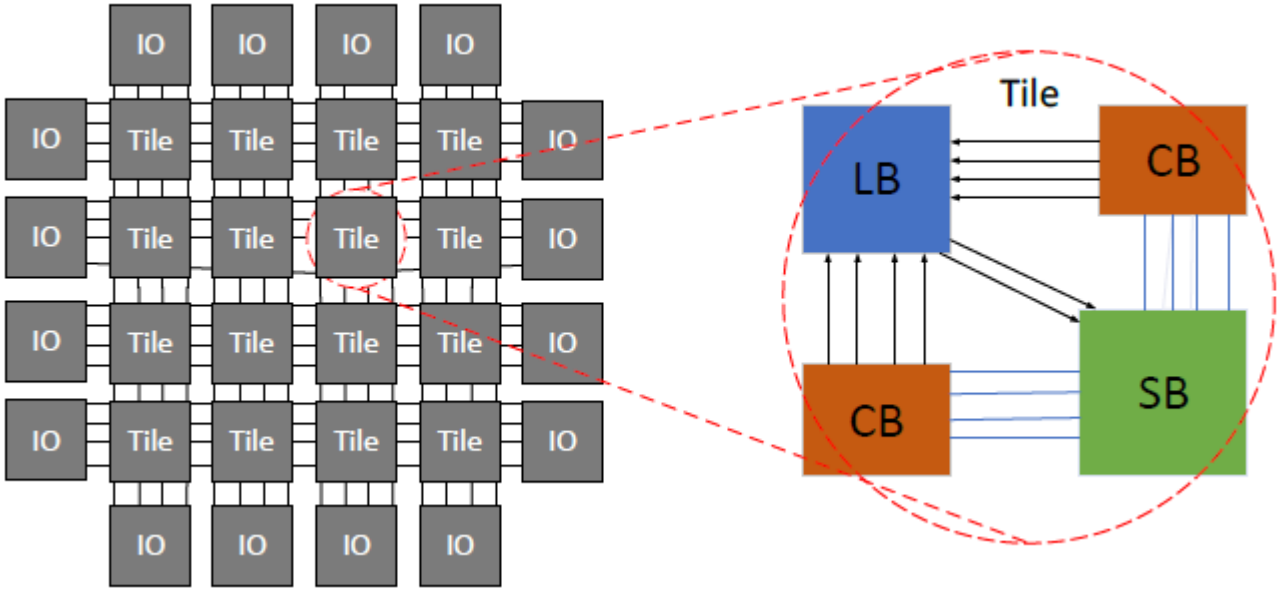


Fig.1 Island-style FPGA architecture

Introduction

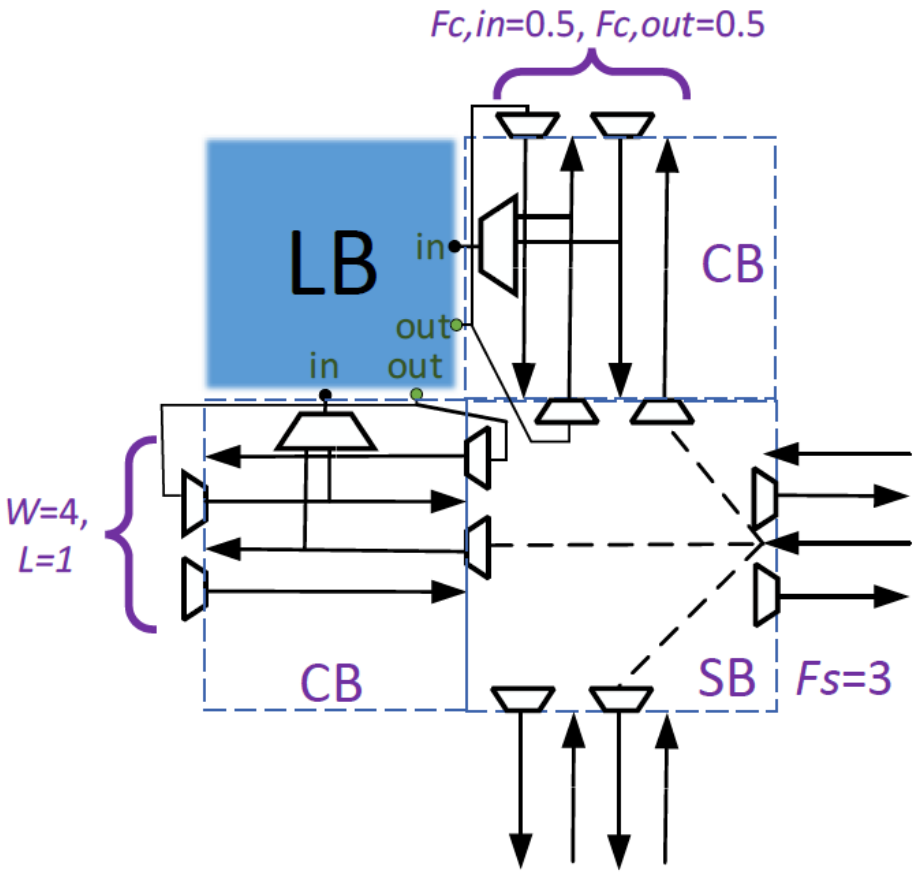


Fig.2 The CB-SB routing architecture

W: Routing Channel Width
L: Wire Length
fc: Connection Block Flexibility
fs: Switch Block Flexibility

Outline

- Introduction
- Related work
- Honeycomb architecture
- Experimental result
- Conclusion & Future work

Related work

- Efficient tiling patterns for FPGA [1]

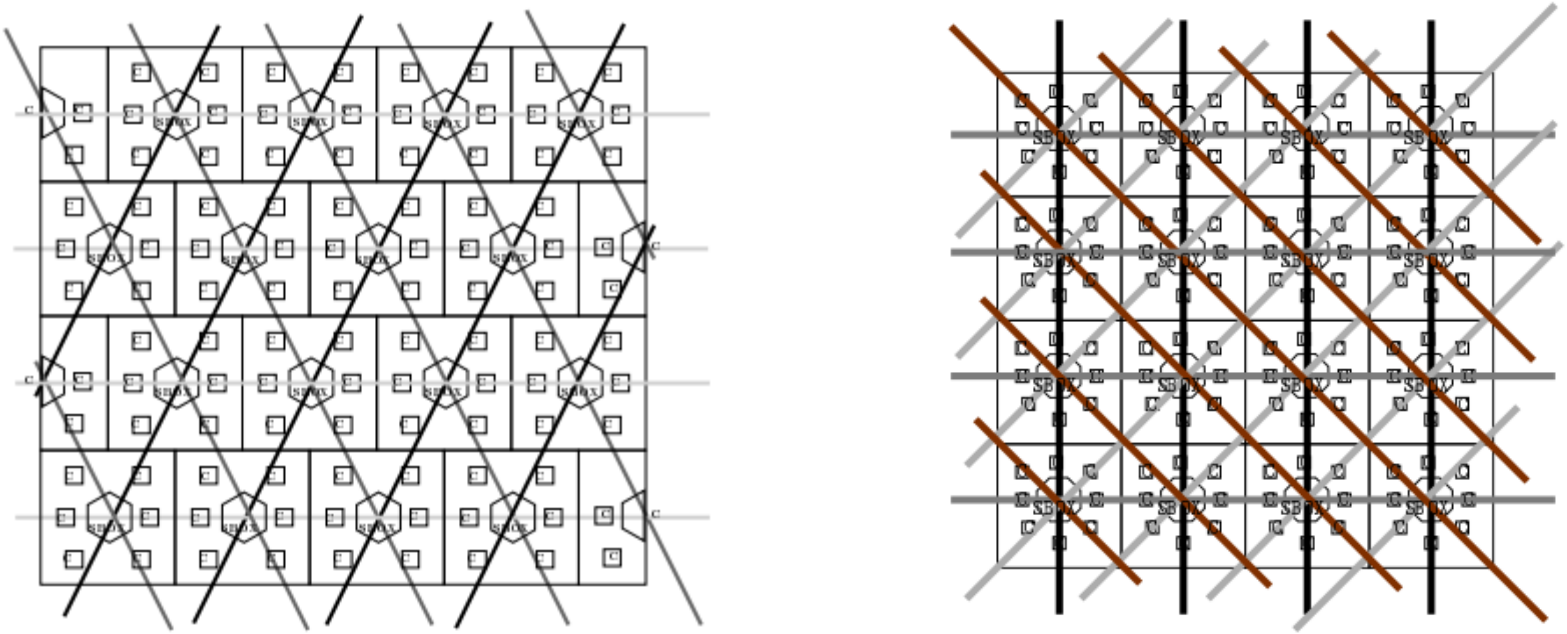


Fig.3 Hexagonal and Octagonal Tiling

- Improved interconnect length with increased area.

[1] S. Chaudhuri, S. Guilley, P. Hoogvorst, and J.-L. Danger, “Efficient tiling patterns for reconfigurable gate arrays,” in Proceedings of the 2008 international workshop on System level interconnect prediction, pp. 11–18, 2008.

Related work

- Diagonal tracks in FPGAs [2]

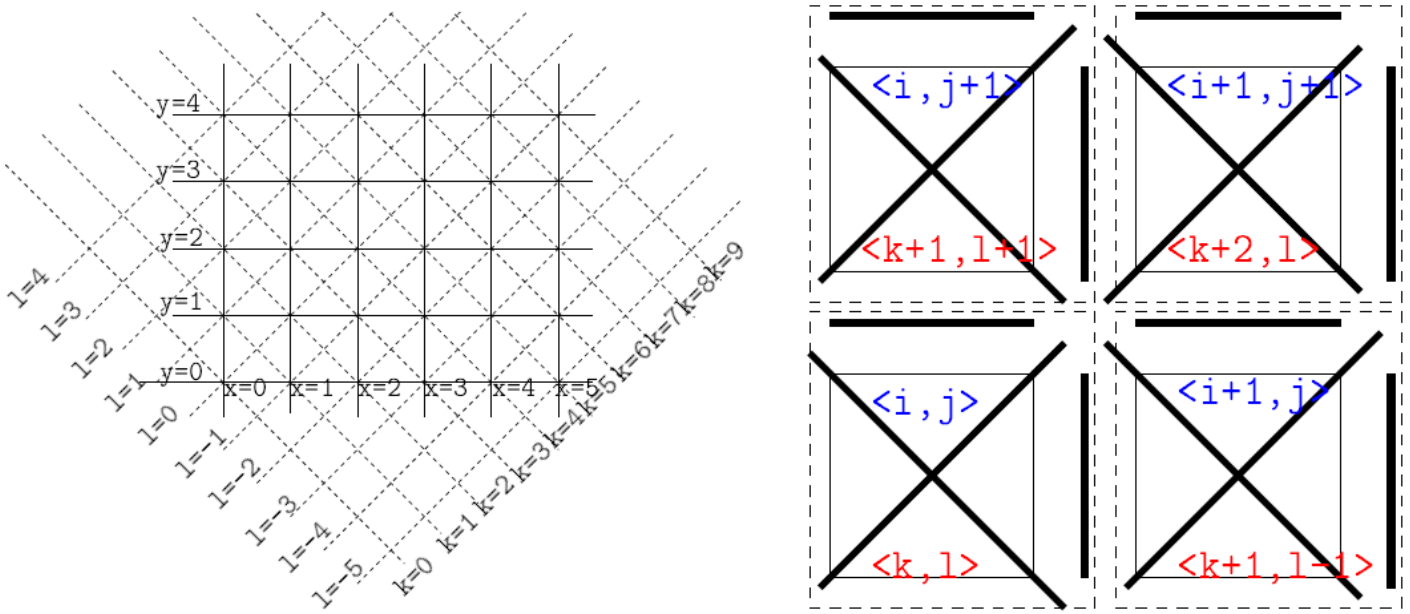


Fig.4 Tile Composition with two new diagonal routing tracks

- Great improvement in wirelength and delay.

[2] S. Chaudhuri, “Diagonal tracks in FPGAs: a performance evaluation,” in Proceedings of the ACM/SIGDA international symposium on Field programmable gate arrays, pp. 245–248, 2009.

Introduction

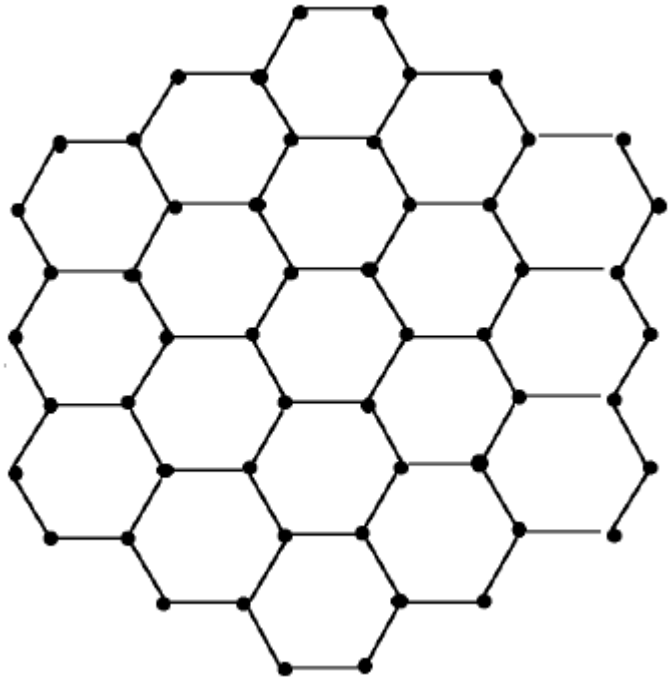


Fig.5 The honeycomb networks [3]

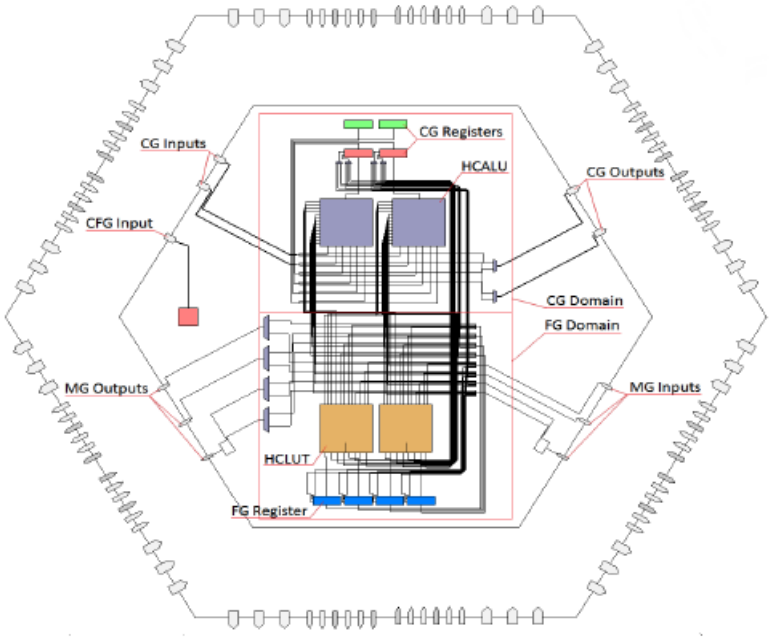


Fig.6 The honeycomb reconfigurable architecture [4]

[3] I. Stojmenovic, “Honeycomb networks: Topological properties and communication algorithms,” IEEE Transactions on parallel and distributed systems, vol. 8, no. 10, pp. 1036–1042, 1997
[4] A. Thomas, M. Ruckauer, and J. Becker, “HoneyComb: A multi-grained dynamically reconfigurable runtime adaptive hardware architecture,” in 2011 IEEE International SOC Conference, pp. 335–340, 2011

Outline

- Introduction
- Related work
- Honeycomb architecture
- Experimental result
- Conclusion & Future work

Honeycomb architecture

Honeycomb FPGA routing architecture:

- Each tile is composed of an LB, an SB and six CBs,
- Each SB has six sides,
- Three kinds of routing channels: X channel, Y channel and Z channel.

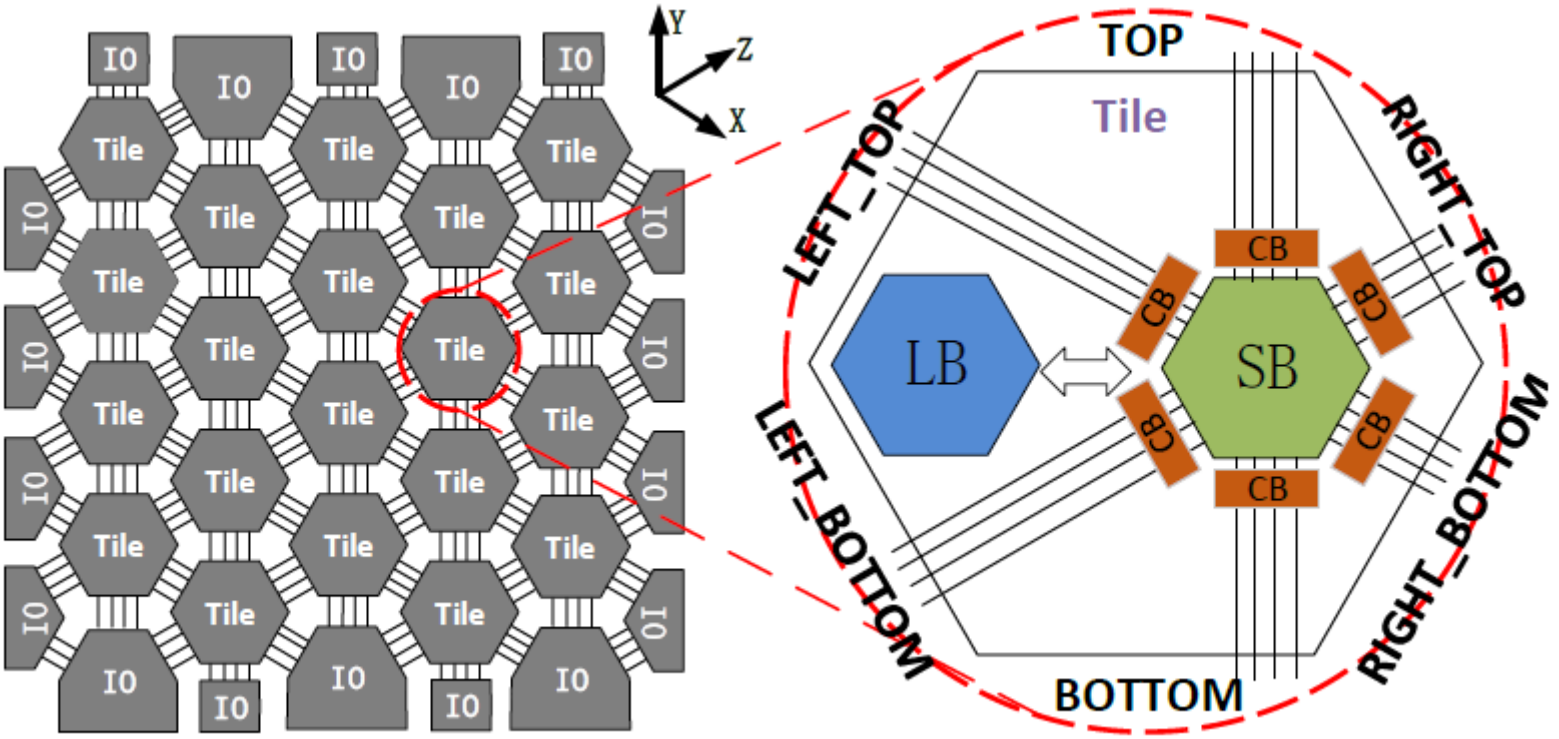
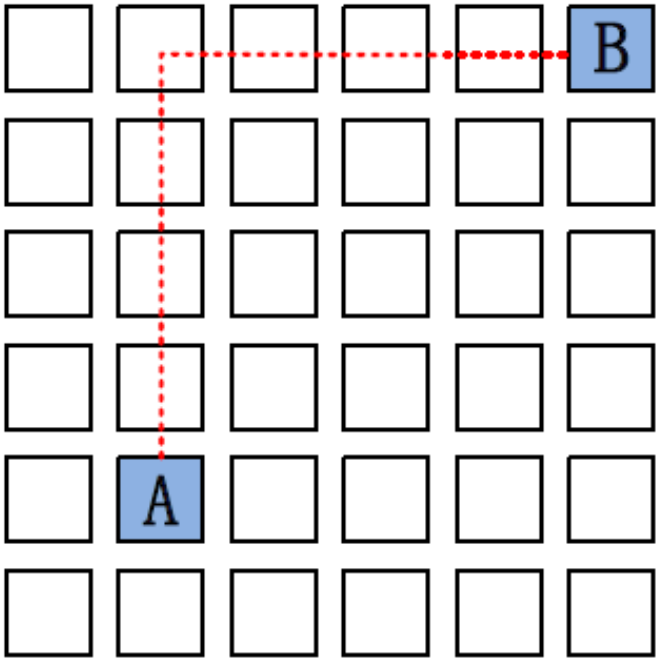


Fig.7 The proposed honeycomb architecture

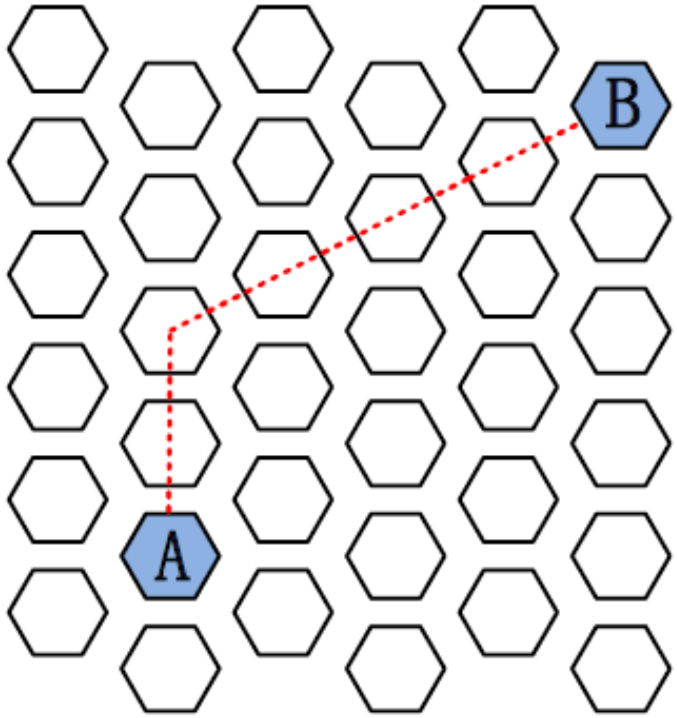
Honeycomb architecture

- Eight length-1 wire segments.



(a) Traditional rectangular architecture

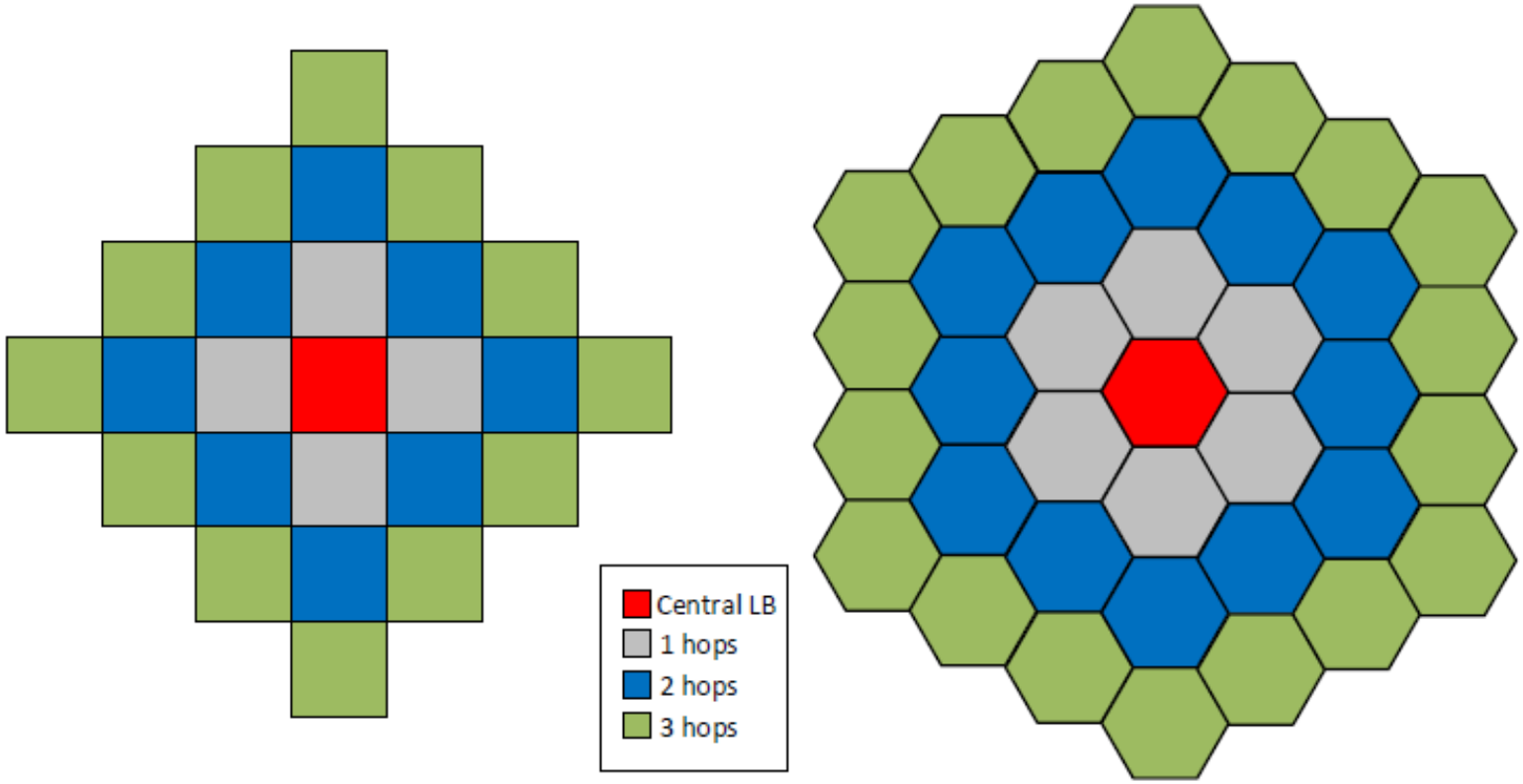
- Six length-1 wire segments.



(b) Honeycomb architecture

Fig.8 One routing path comparison

Honeycomb architecture



(a) Traditional rectangular architecture (b) Honeycomb architecture

Fig.9 The hops distribution comparison with length-1 wires

Honeycomb architecture

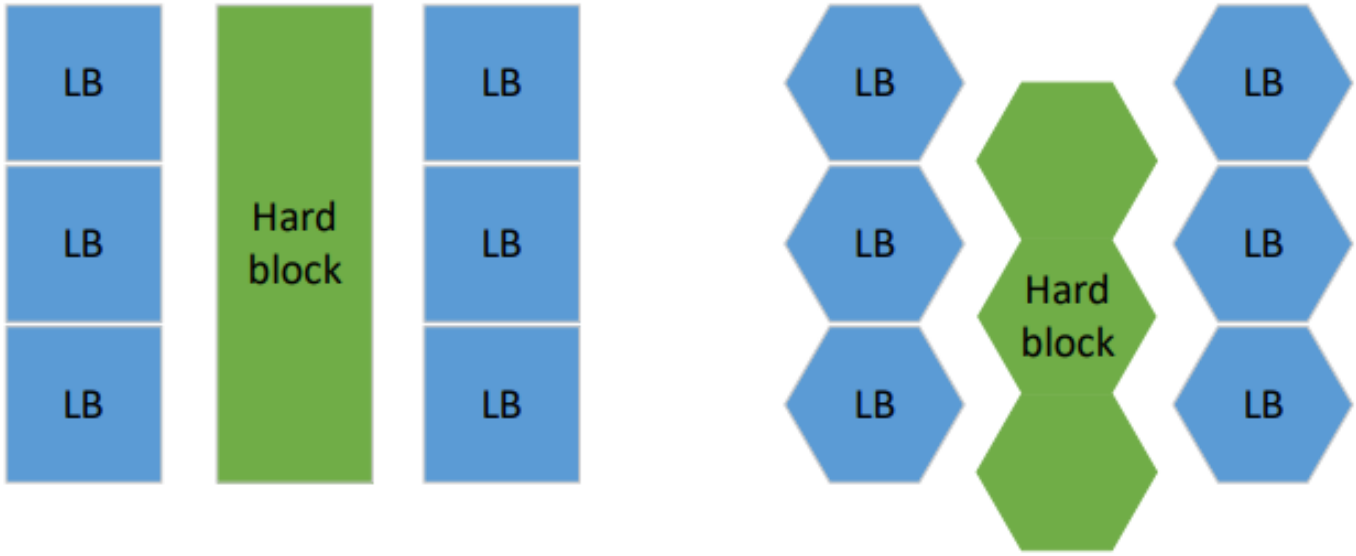
Table I. comparison between the routing resources of the traditional architecture and the honeycomb architecture

Hops	Number of LBs reachable	
	traditional architecture	honeycomb architecture
1	4	6
2	8	12
3	12	18
Total	24	36

- the honeycomb architecture can connect to 1.5 times as many LBs as the traditional rectangular architecture can connect to through the same hops.

Honeycomb architecture

- Heterogeneous Blocks



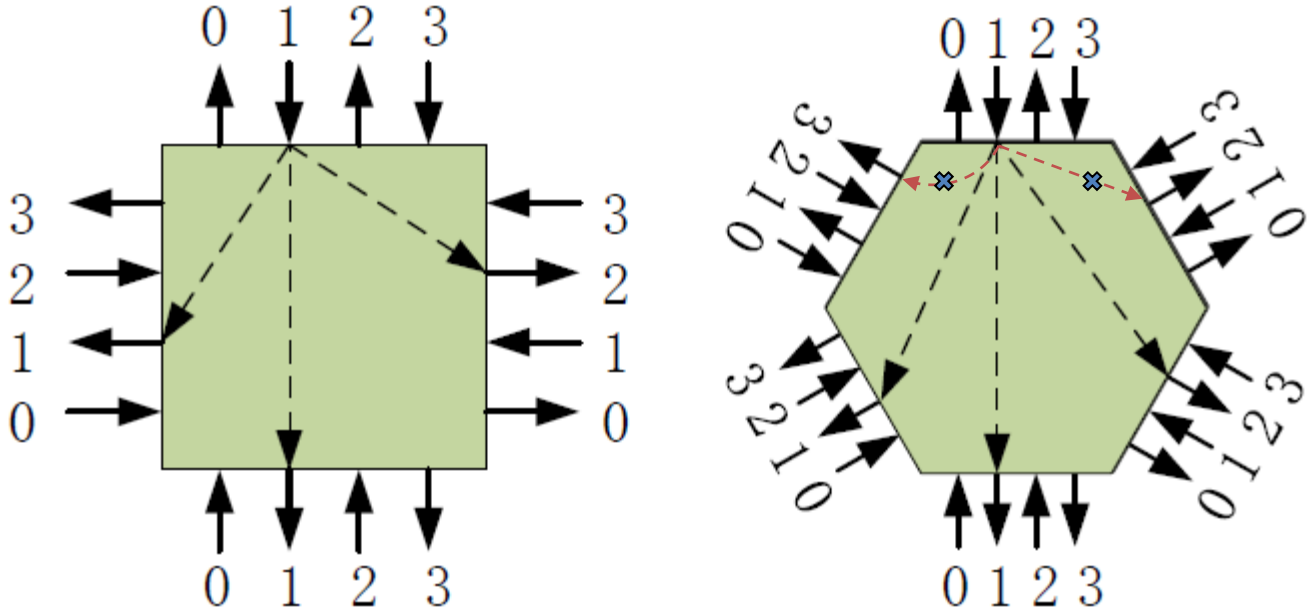
(a) Traditional rectangular architecture (b) Honeycomb architecture

Fig.10 The hard blocks comparison

Honeycomb architecture

➢ SB enhancement

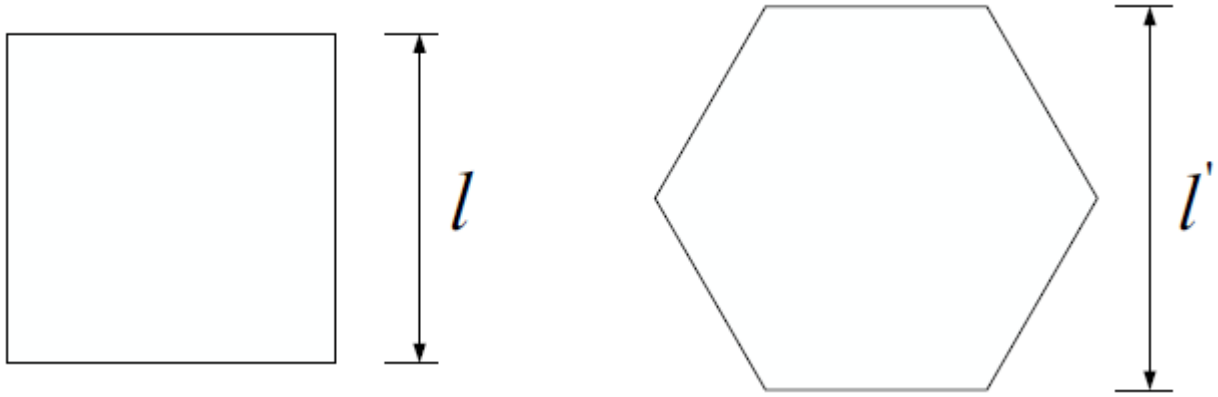
- Fs = 3
- No connections between the wires and its two neighboring sides.



(a) Traditional rectangular architecture (b) Honeycomb architecture

Fig.11 The Wilton SB pattern

Honeycomb architecture



(a) a square with side length l (b) a regular hexagon with height l'

Fig.12 The comparison of a square and a regular hexagon

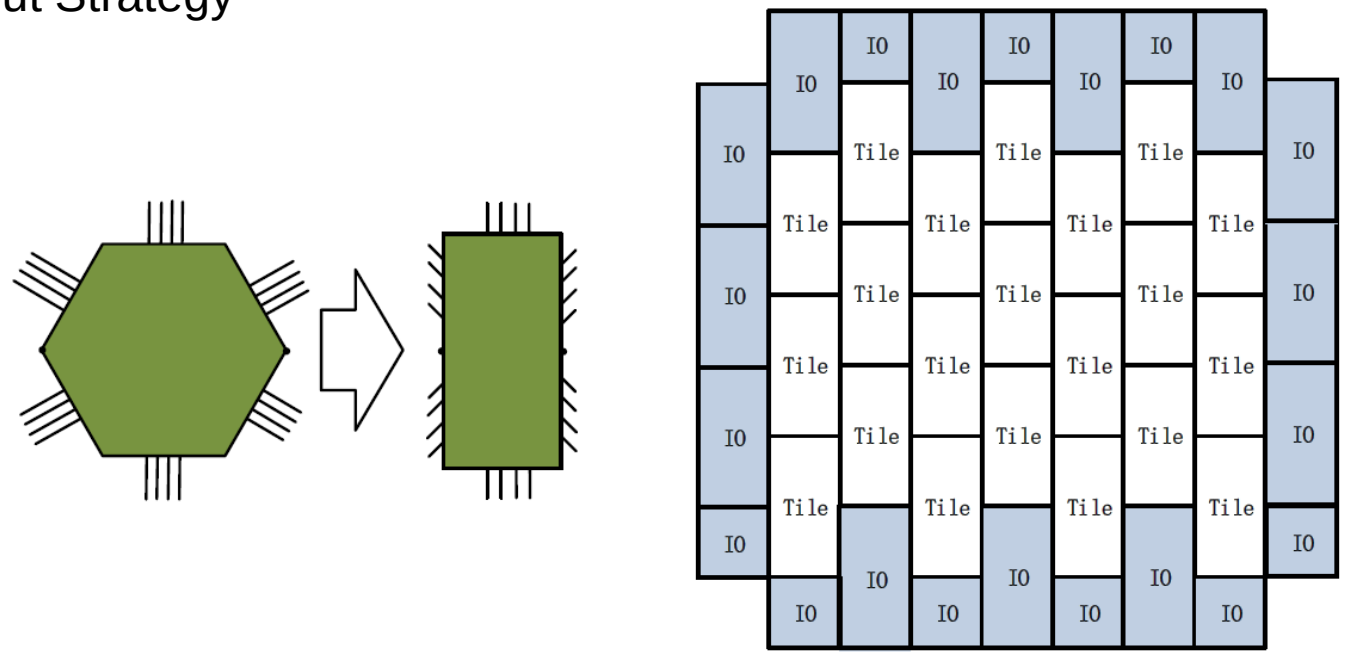
$$S = l^2 \tag{1}$$

$$S' = 6 \times \frac{l'}{\sqrt{3}} \times \frac{l'}{2} \times \frac{1}{2} = \frac{\sqrt{3}}{2} l'^2 \tag{2}$$

$$l' = 1.07l \tag{3}$$

Honeycomb architecture

- Layout Strategy



(a) (b)

Fig.13 The layout strategy of the honeycomb architecture. (a) The hexagon becomes a rectangle with an aspect ratio of 2. (b) The possible layout.

Honeycomb architecture

- Router lookahead enhancement

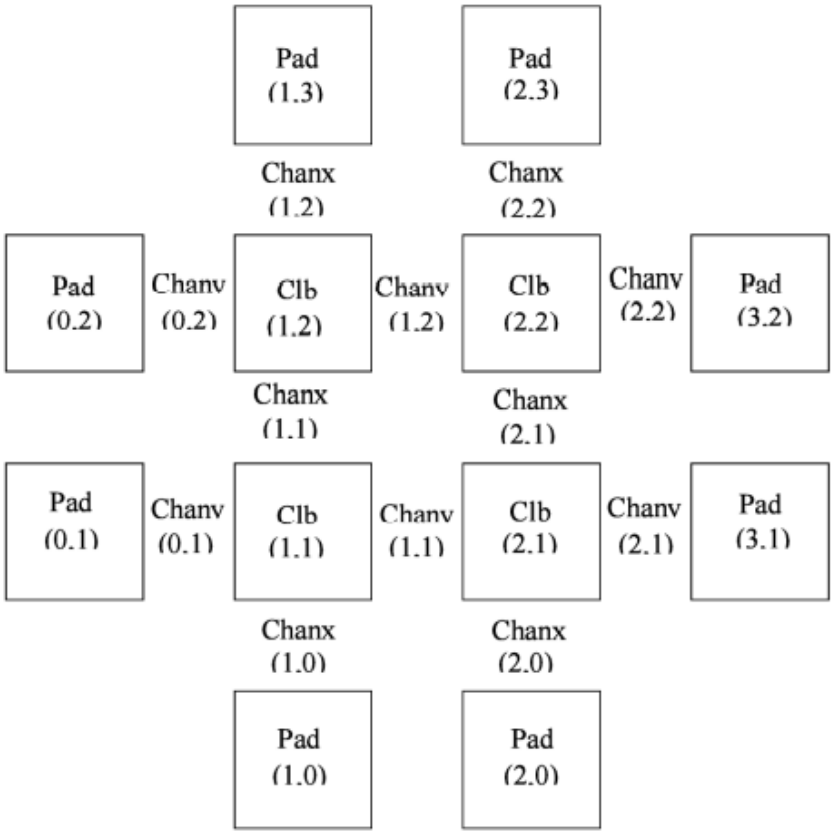
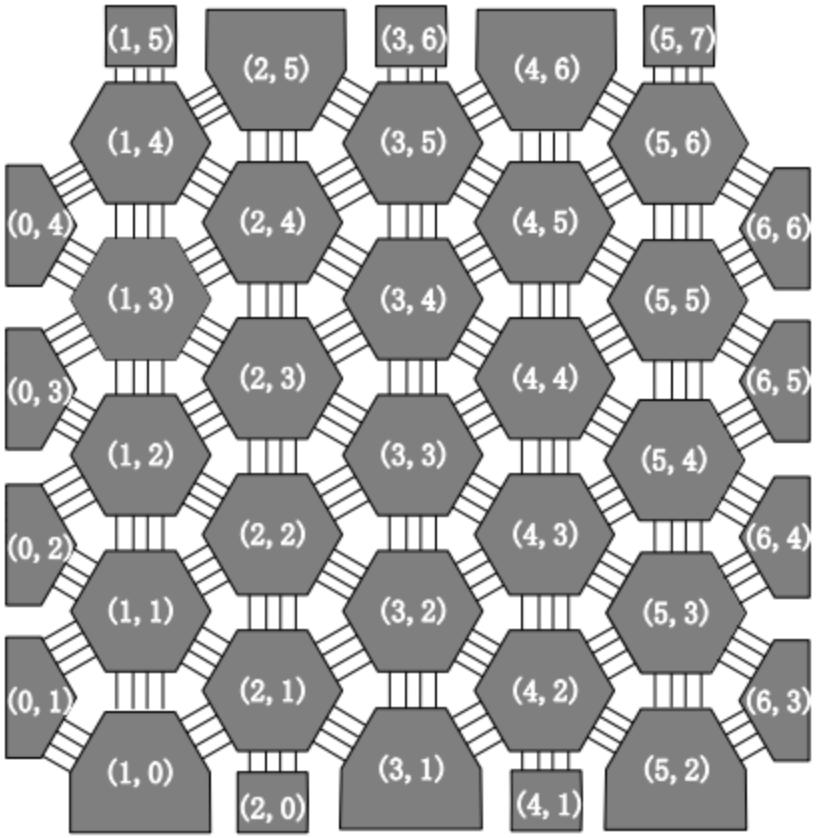


Fig.14 The coordinate system used by VPR

Honeycomb architecture

- Router lookahead enhancement



$$x = x'$$

$$y = \begin{cases} y' & x < 3 \\ y' + \lfloor (x' - 1)/2 \rfloor & x \geq 3 \end{cases}$$

$$n = \begin{cases} \left\lceil \frac{||\Delta x| - |\Delta y||}{L} \right\rceil + \left\lceil \frac{\min(|\Delta x|, |\Delta y|)}{L} \right\rceil & \Delta x \cdot \Delta y \geq 0 \\ \left\lceil \frac{|\Delta x|}{L} \right\rceil + \left\lceil \frac{|\Delta y|}{L} \right\rceil & \Delta x \cdot \Delta y < 0 \end{cases}$$

Fig.15 The new coordinate system

Outline

- Introduction
- Related work
- Honeycomb architecture
- Experimental result
- Conclusion & Future work

Experimental result

Table II. Baseline architecture parameters

LB	ten 6-input fracturable LUTs
DSP	36×36 fracturable multipliers
Memories	configurable 32K block RAMs
SB	Wilton
L	1
W	300
Fc,in	0.1
Fc,out	0.1
Fs	3

Experimental result

Table III. Comparison of W_{min} between honeycomb architecture and rectangular architecture

Circuit	W_{min}		
	HC	REC	Ratio
arm_core	64	108	88.9%
bgm	38	64	89.1%
blob_merge	38	60	95.0%
boundtop	16	24	100.0%
ch_intrinsics	16	26	92.3%
diffeq1	22	44	75.0%
diffeq2	22	34	97.1%
LU8PEEng	52	90	86.7%
LU32PEEng	80	120	100.0%
mcml	52	78	100.0%
mkDelayWorker32B	16	20	120.0%
mkPktMerge	20	26	115.4%
mkSMAdapter4B	30	48	93.8%
or1200	38	70	81.4%
raygentop	22	42	78.6%
sha	32	52	92.3%
stereovision0	26	46	84.8%
stereovision1	34	70	72.9%
stereovision2	56	92	91.3%
stereovision3	16	26	92.3%
Av. Improvement		**7.7%**	

[a] Ratio is the results of $1.5W_{min}$ in the honeycomb architecture divided by W_{min} in rectangular architecture.

- Fc = 0.15,
- Length-1 wires
- HC: honeycomb architecture
- REC: rectangular architecture

Experimental result

Table IV. Result of honeycomb architecture compared with rectangular architecture

Circuit	Routed Wirelength			Total Area (10^6)			Critical Path Delay (ns)			Area-Delay Product (10^6)		
	HC	REC	Ratio	HC	REC	Ratio	HC	REC	Ratio	HC	REC	Ratio
arm_core	139072	154558	90.0%	82.67	83.10	99.5%	17.87	21.11	84.7%	1477.12	1753.88	84.2%
bgm	180943	193787	93.4%	136.57	137.15	99.6%	16.48	18.23	90.4%	2250.74	2500.12	90.0%
blob_merge	43967	47704	92.2%	39.17	39.45	99.3%	7.26	9.19	79.0%	284.24	362.57	78.4%
boundtop	602	591	101.9%	5.54	5.65	98.2%	1.67	2.12	78.5%	9.25	12.00	77.1%
ch_intrinsics	509	613	83.1%	4.60	4.69	98.2%	2.35	2.27	103.3%	10.81	10.65	101.5%
diffeq1	4365	4982	87.6%	6.86	6.97	98.4%	13.26	14.17	93.6%	90.88	98.71	92.1%
diffeq2	3165	3674	86.1%	6.86	6.97	98.4%	10.69	11.72	91.2%	73.26	81.68	89.7%
LU8PEEng	203701	218796	93.1%	131.02	131.58	99.6%	68.53	79.64	86.1%	8979.41	10478.49	85.7%
LU32PEEng	913439	1012027	90.3%	457.67	458.84	99.7%	66.51	81.30	81.8%	30440.53	37302.41	81.6%
mcml	402294	435223	92.4%	378.99	380.01	99.7%	56.18	65.84	85.3%	21291.85	25020.39	85.1%
mkDelayWorker32B	12295	11894	103.4%	108.27	108.78	99.5%	9.69	10.15	95.5%	1049.50	1104.06	95.1%
mkPktMerge	7808	7757	100.7%	31.61	31.86	99.2%	4.93	5.31	92.8%	155.76	169.10	92.1%
mkSMAdapter4B	7829	8177	95.7%	15.26	15.43	98.9%	5.43	5.51	98.6%	82.94	85.03	97.5%
or1200	28188	31937	88.3%	29.45	29.69	99.2%	12.18	12.92	94.3%	358.78	383.62	93.5%
raygentop	9731	12416	78.4%	18.79	18.98	99.0%	3.70	4.38	84.4%	69.46	83.17	83.5%
sha	12681	14026	90.4%	13.53	13.69	98.8%	9.74	12.09	80.5%	131.70	165.53	79.6%
stereovision0	33432	37729	88.6%	48.13	48.45	99.3%	2.84	3.06	92.6%	136.46	148.43	91.9%
stereovision1	65505	83256	78.7%	60.91	61.28	99.4%	5.29	5.90	89.7%	322.50	361.74	89.2%
stereovision2	371172	437600	84.8%	330.49	331.45	99.7%	15.12	18.70	80.9%	4997.21	6196.53	80.6%
stereovision3	284	342	82.9%	1.11	1.15	96.6%	1.89	2.19	86.1%	2.11	2.53	83.2%
Av. Improvement		**9.9%**			**1.0%**			**11.5%**			**12.4%**	

- Fc = 0.15
- W = 200
- Length-1 wires

Experimental result

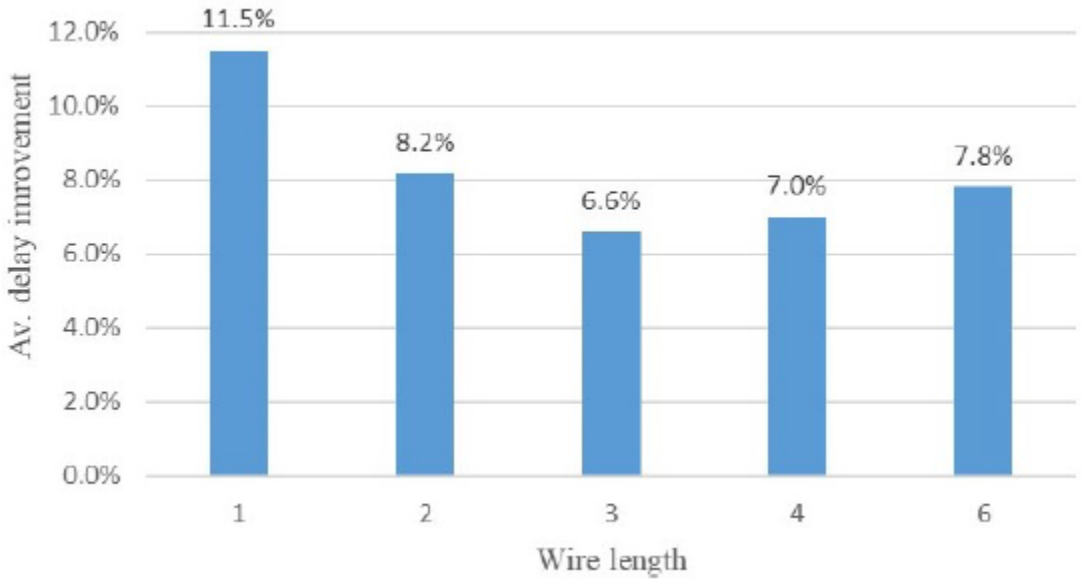


Fig.16 The delay improvement of the honeycomb architecture with different wire lengths.

- The honeycomb architecture with length-1 wire segments improve delay by 11.5%.

Outline

- Introduction
- Related work
- Honeycomb architecture
- Experimental result
- Conclusion & Future work

Conclusion & Future work

Conclusion

- A hexagon-based honeycomb routing architecture is proposed and evaluated in VTR 8.
- The honeycomb architecture can improve the critical path delay by 11.5% and achieve area-delay product savings by 12.4% on average.

Future work

- Explore the placement and routing algorithms.
- Explore the routing channel segmentation with different lengths and SB pattern design.
- Explore the fabrication effect of the honeycomb architecture.

THANK YOU