GIB: A Novel Unidirectional Interconnection Architecture for FPGA

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Outline

- Introduction
- Related work
- GIB architecture
- Experimental result
- Conclusion & Future work

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Introduction

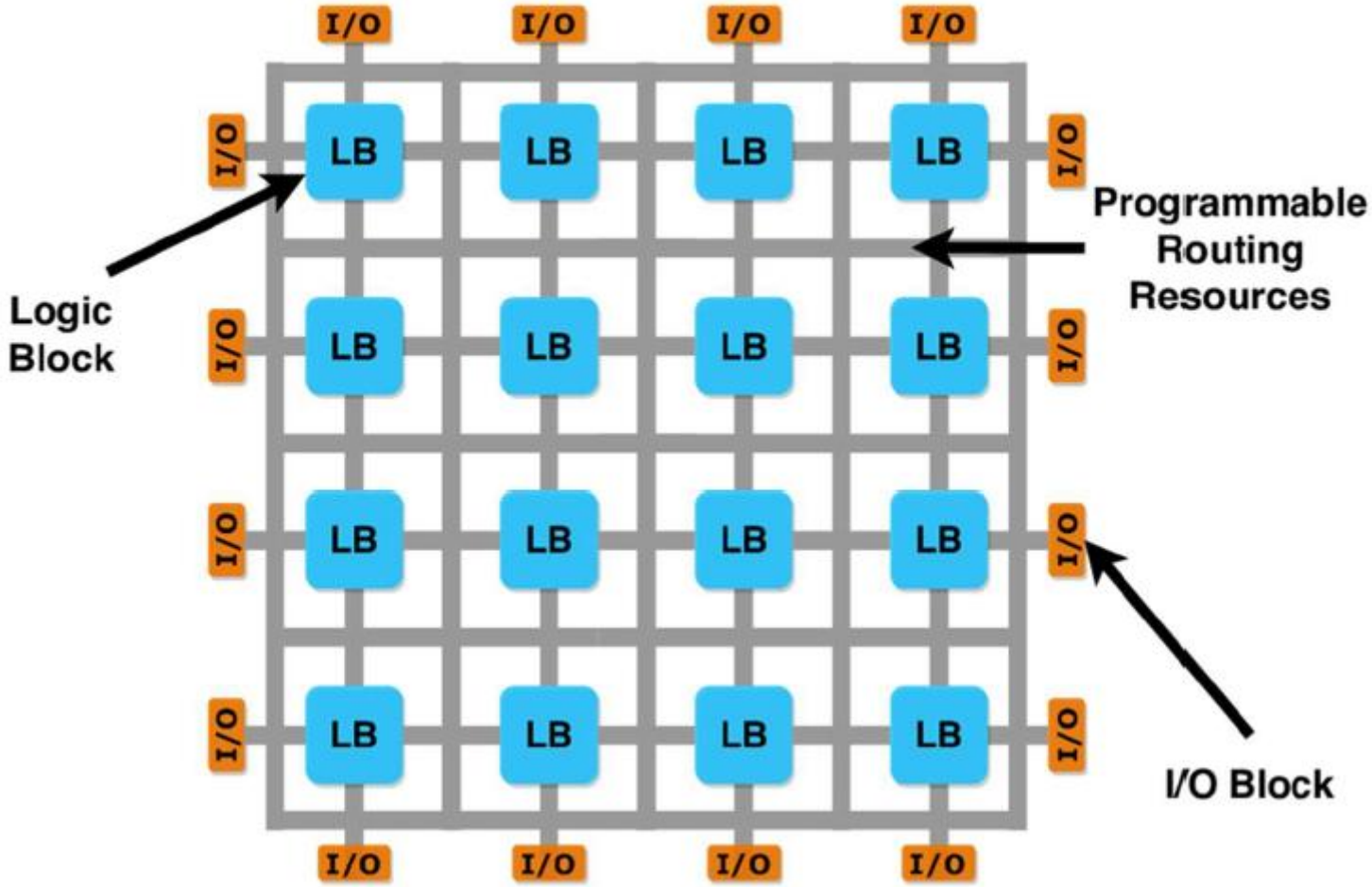

Fig.1 The architecture of island-style FPGAs [1]

[1] V. Betz, J. Rose, and A. Marquardt, Architecture and CAD for Deep-Submicron FPGAs. Kluwer Academic Publishers, 1999.

Introduction

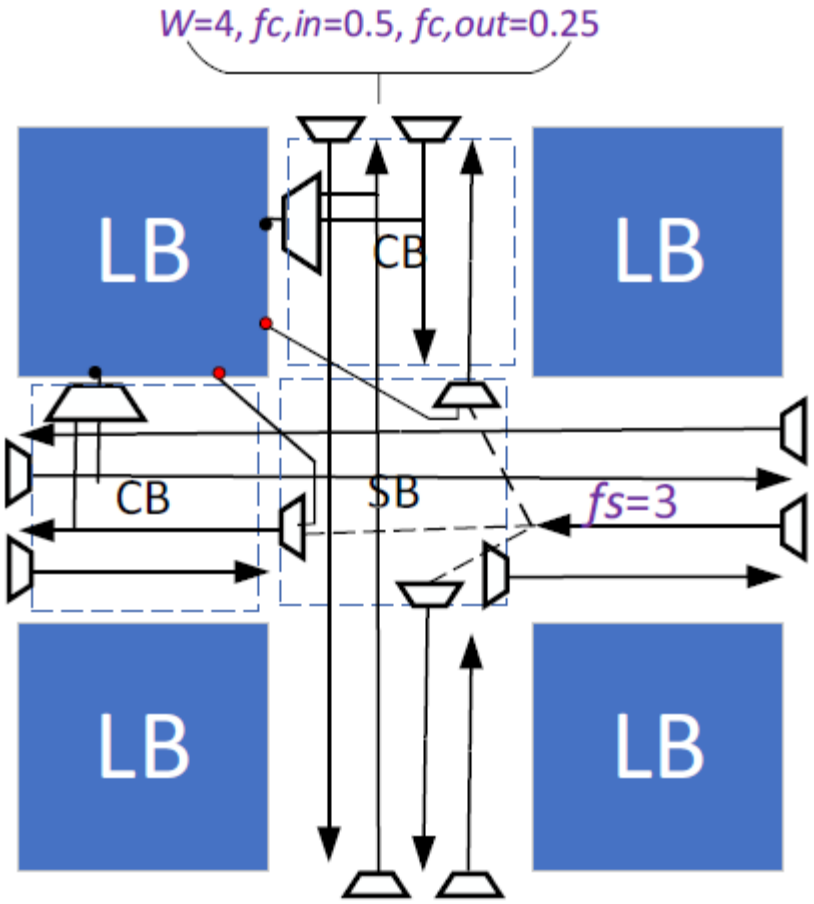

Fig.2 The CB-SB routing architecture

LB: **L**ogic **B**lock
CB: **C**onnection **B**lock
SB: **S**witch **B**lock
W: Routing Channel Width
L: Wire length
fc: Connection Block Flexibility
fs: Switch Block Flexibility

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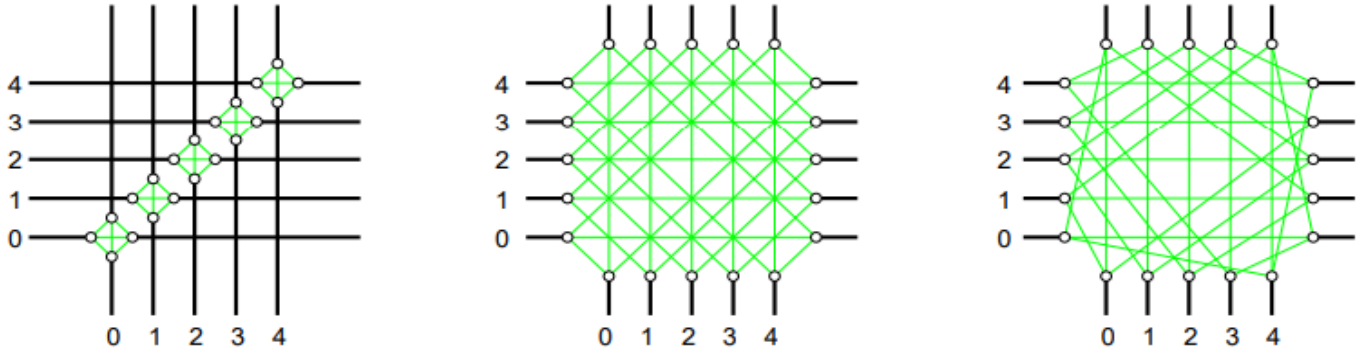
Related work

SB has a large impact on the FPGA flexibility and performance.



Disjoint [2] Universal [3] Wilton [4]

Fig.3 SB pattern

[2] G.F. Lemieux, S.D. Brown and D. Vranesic, "On Two-step Routing for FPGAS", ISPD '97, pp. 60-66, April 1997.
[3] Y.-W. Chang et al., Universal switch blocks for FPGA design, ACM Transactions Design Automation of Electronic Systems, vol. 1, pp. 80–101, 1996 .
[4] S. Wilton et al., Architecture and algorithms for Field-Programmable Gate Arrays with embedded memory, PhD thesis, University of Toronto, 1997.

Related work

- CS-Box (Connection-Switch Box):
  an LB pin can connect to the wire segments on the three sides of a CS-Box.
- GSB (General Switch Box):
  an LB pin can connect to the wire segments on the four sides of a GSB.

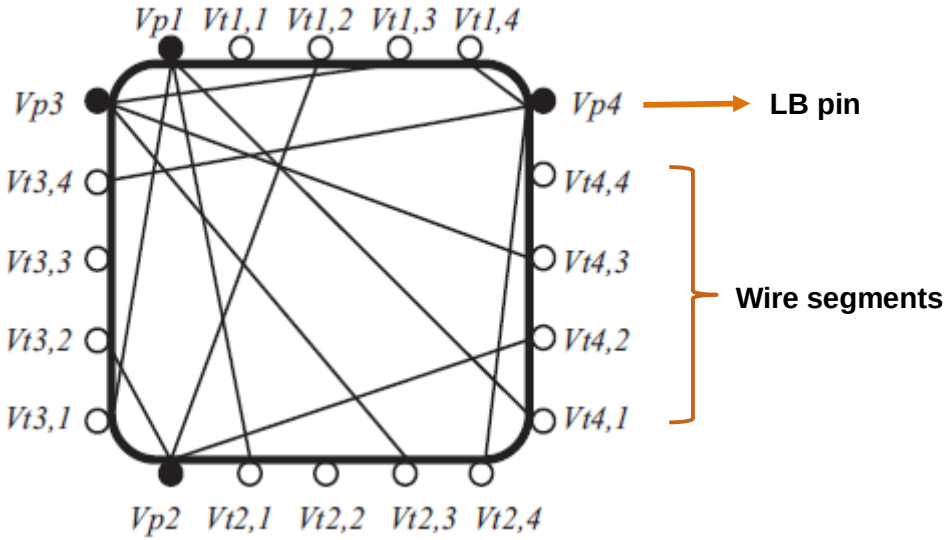


Fig.4 CS-Box [5]

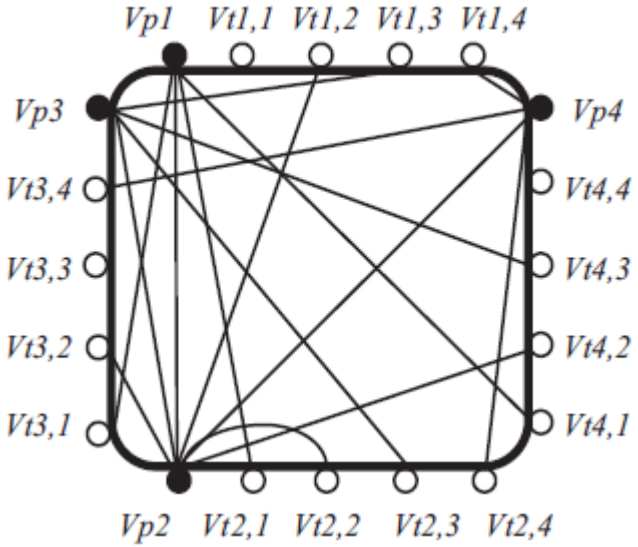


Fig.5 GSB [6]

[5] C. Zhou, R. Cheung, and Y.-L Wu. “What if merging connection and switch boxes -- an experimental revisit on FPGA architectures,” IEEE International Conference on Communications, Circuits and Systems, 2004, 1295 -1299

[6] K. Ma, L. Wang, X. Zhou, S. Tan and J. Tong, “General switch box modeling and optimization for FPGA routing architectures,” IEEE International Conference on Field-Programmable Technology (FPT), 2010, pp. 320–323.

Related work

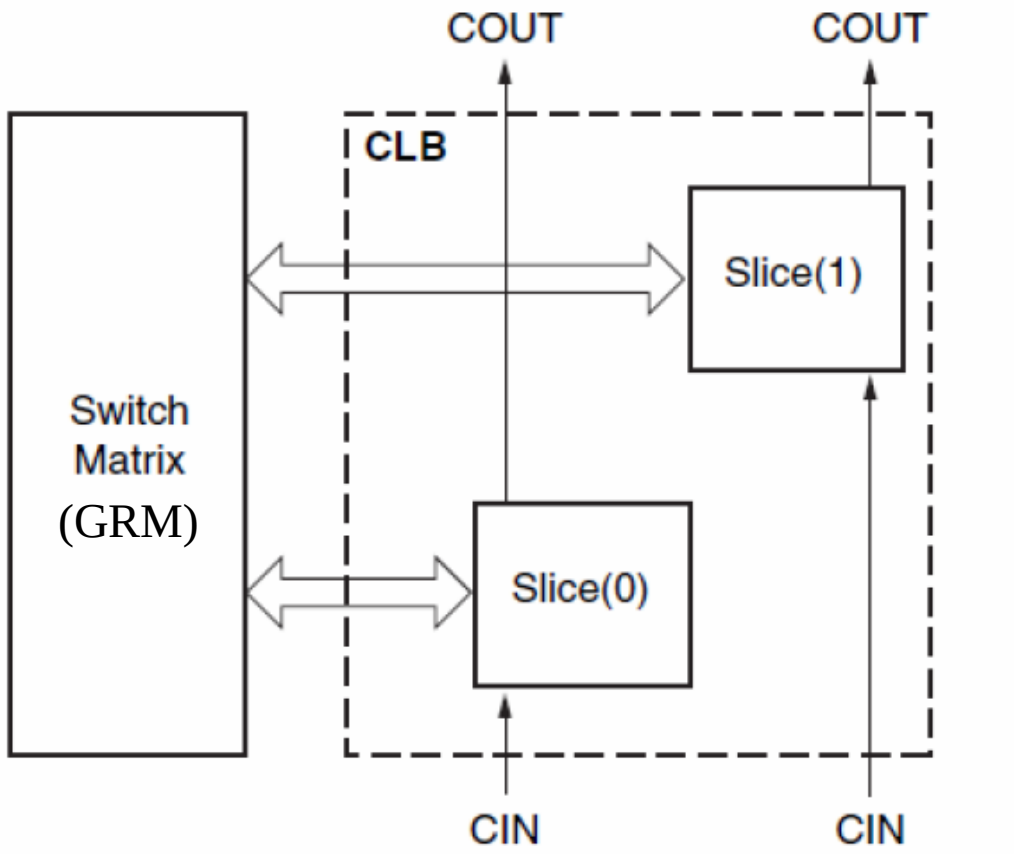


Fig.6 GRM in Virtex-5

- The general routing matrix (GRM)[7] provides an array of routing switches.
- Each programmable element is tied to a switch matrix.

[7] Virtex-5 Family Overview, Xilinx, DS100 (v5.1) August 21, 2015

Related work

HARP (Hard-wired Routing Pattern) :

a mixture of hard-wired and traditional flexible switches.

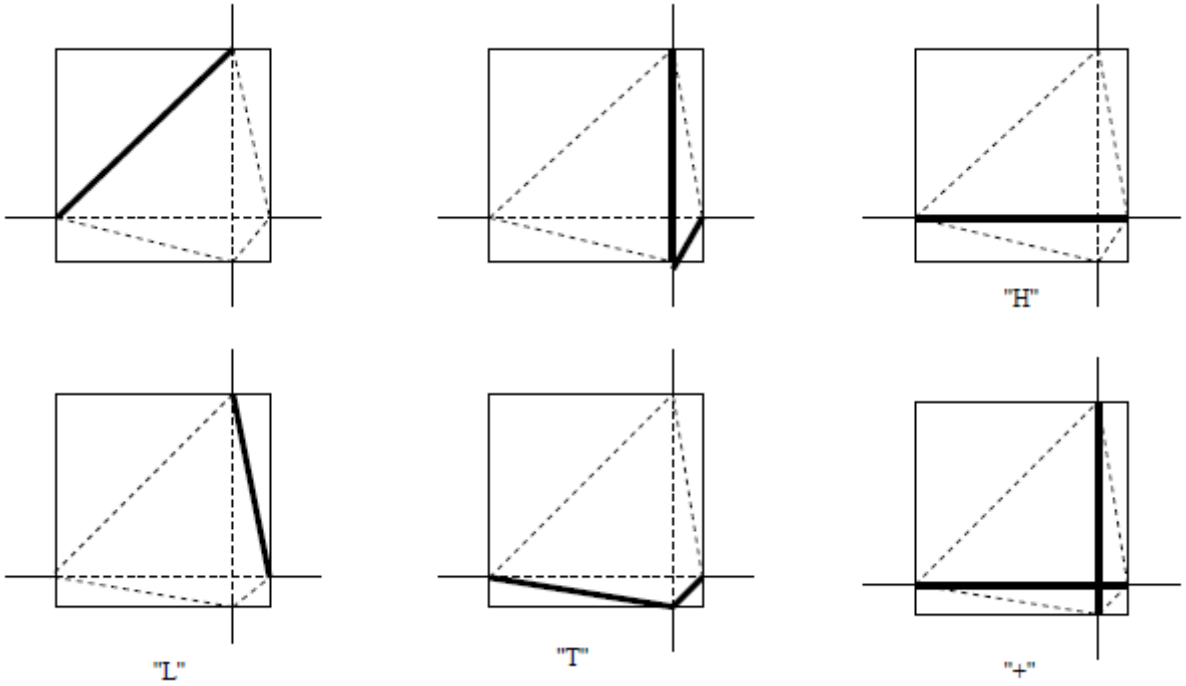


Fig.7 Some possible hard-wired patterns [8]

[8] S. Sivaswamy et al., “HARP: hard-wired routing pattern FPGAs”, 13th international symposium on Field-programmable gate arrays. ACM, 2005, pp. 21–29.

Related work

Bent Routing Pattern:

bent wires can span in both vertical and horizontal channels without switch.

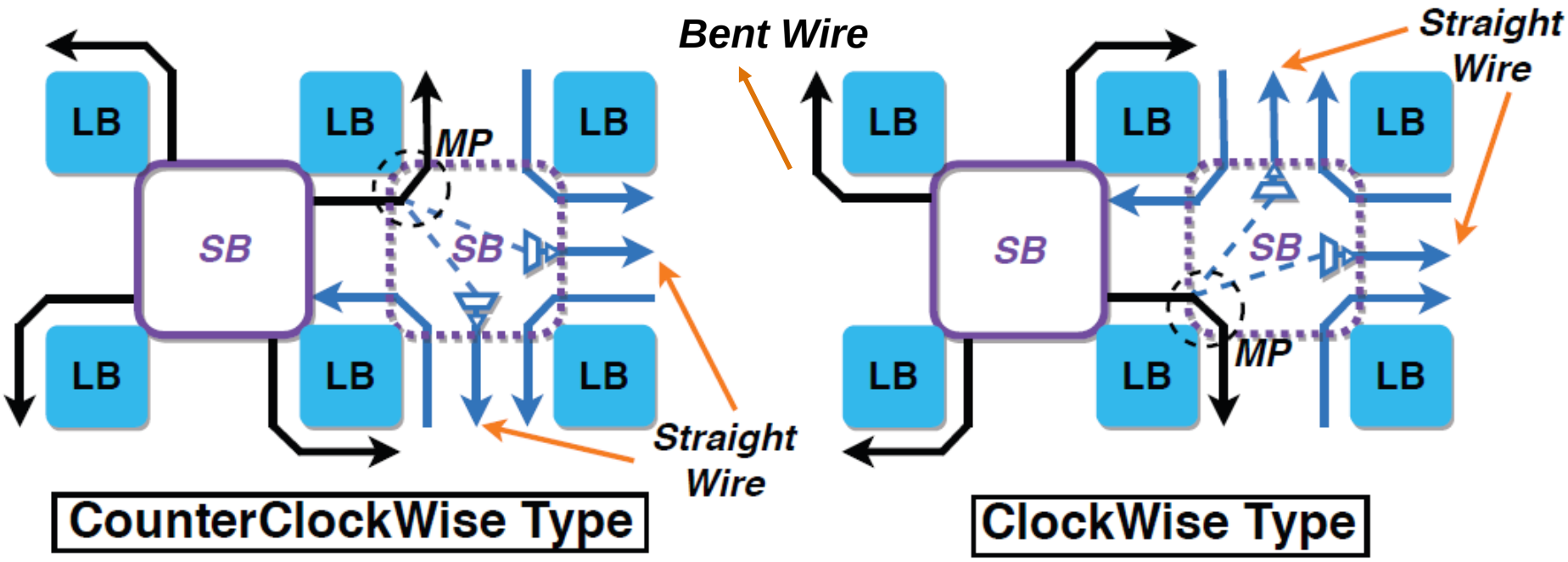


Fig.8 The architecture with bent wires [9]

[9] X. Sun, H. Zhou and L. Wang, “Bent routing pattern for FPGA”, 29th International Conference on Field Programmable Logic and Applications (FPL), 2019, pp. 9–16.

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GIB architecture

GIB(General Interconnection Block):

- an LB can connect to four adjacent GIBs without programmable switches,
- a GIB has four adjacent LBs.

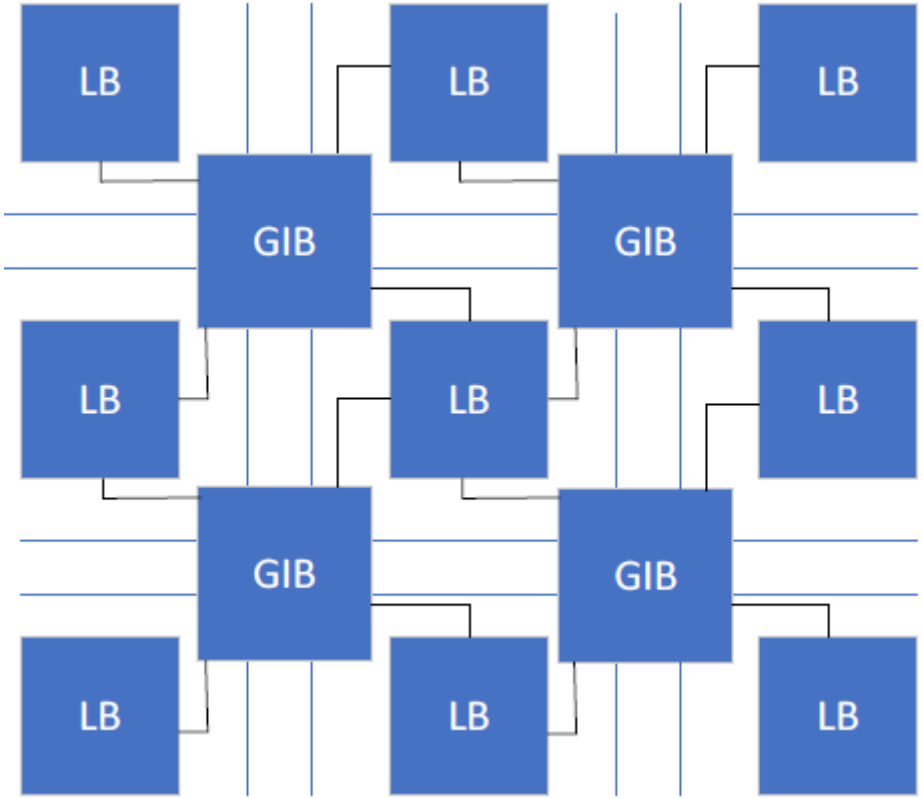


Fig.9 GIB architecture

GIB architecture

- An LB pin can only connect to one adjacent routing channel.
- An LB pin can connect to the routing channels on the four sides.

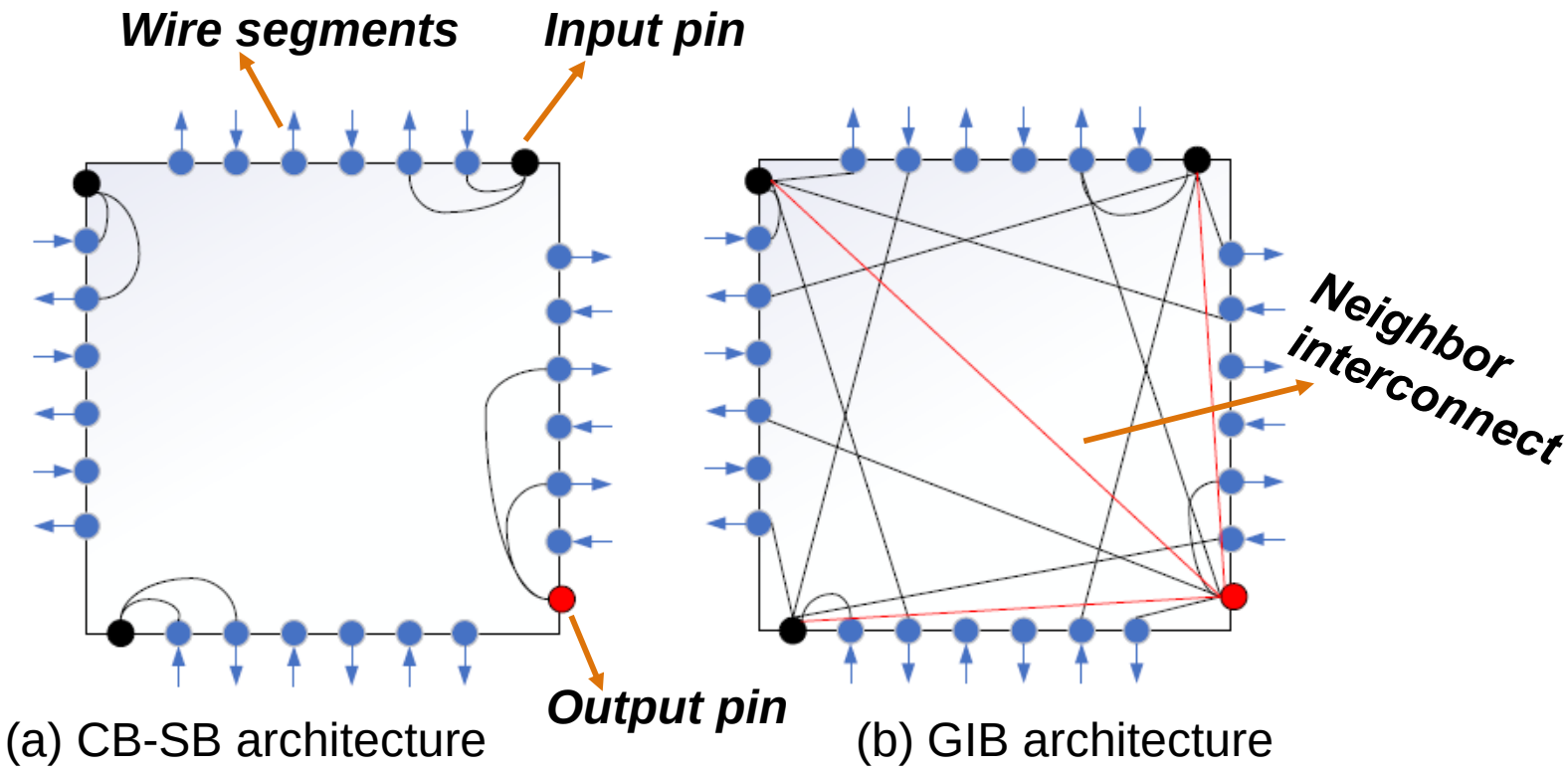
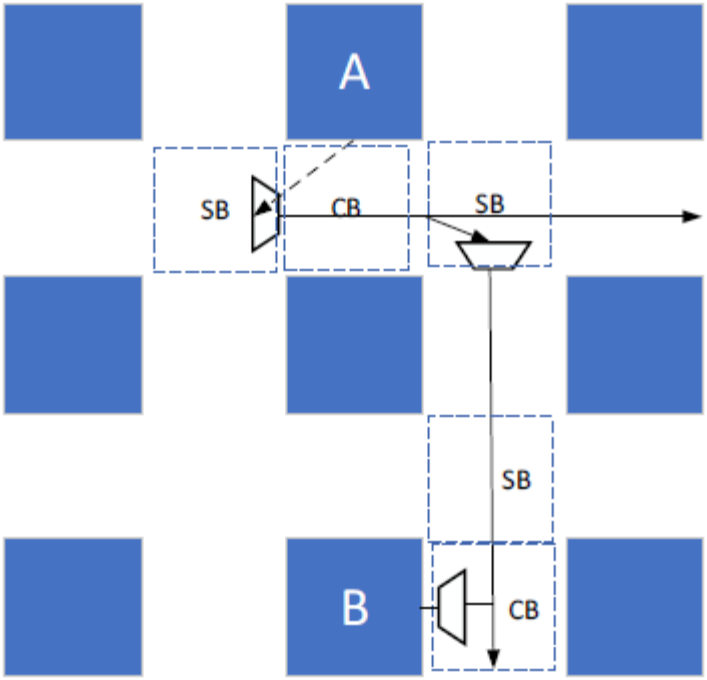


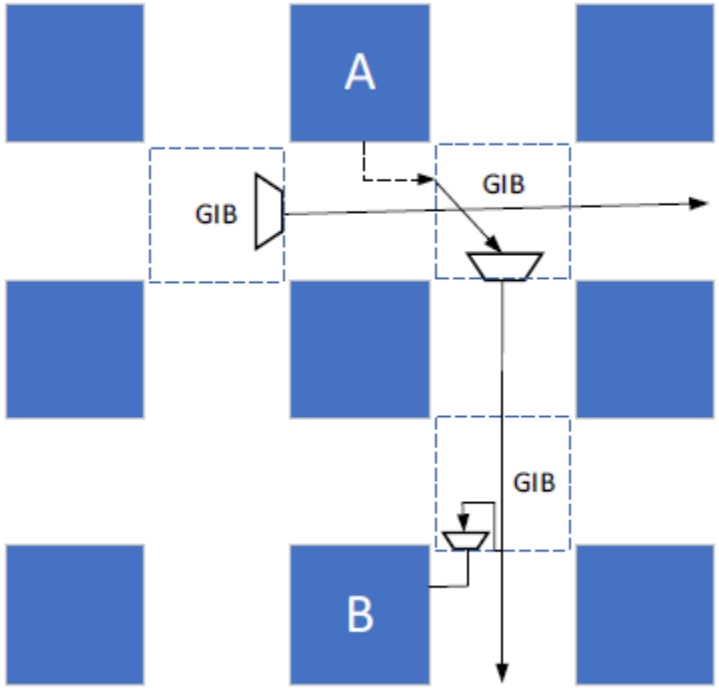
Fig.10 Comparison of CB-SB and GIB modeling

GIB architecture

- Pass through 3 muxes
- Pass through 2 muxes



(a) CB-SB architecture



(b) GIB architecture

Fig.11 The routing path compared CB-SB with GIB architecture

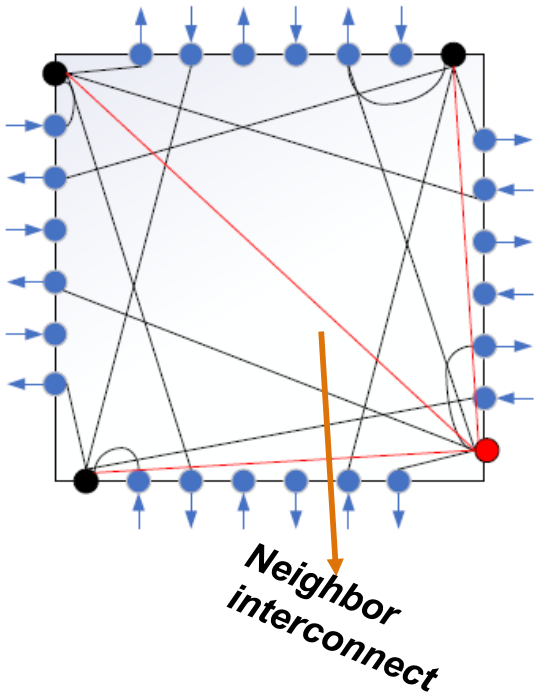
GIB architecture

The connections in GIB can be divided into three types:

1. Between LB pins and wire segments: (*fc*)
2. Between different wire segments: (*fs*)
3. Between LB output pins and LB input pins: (*fn*)

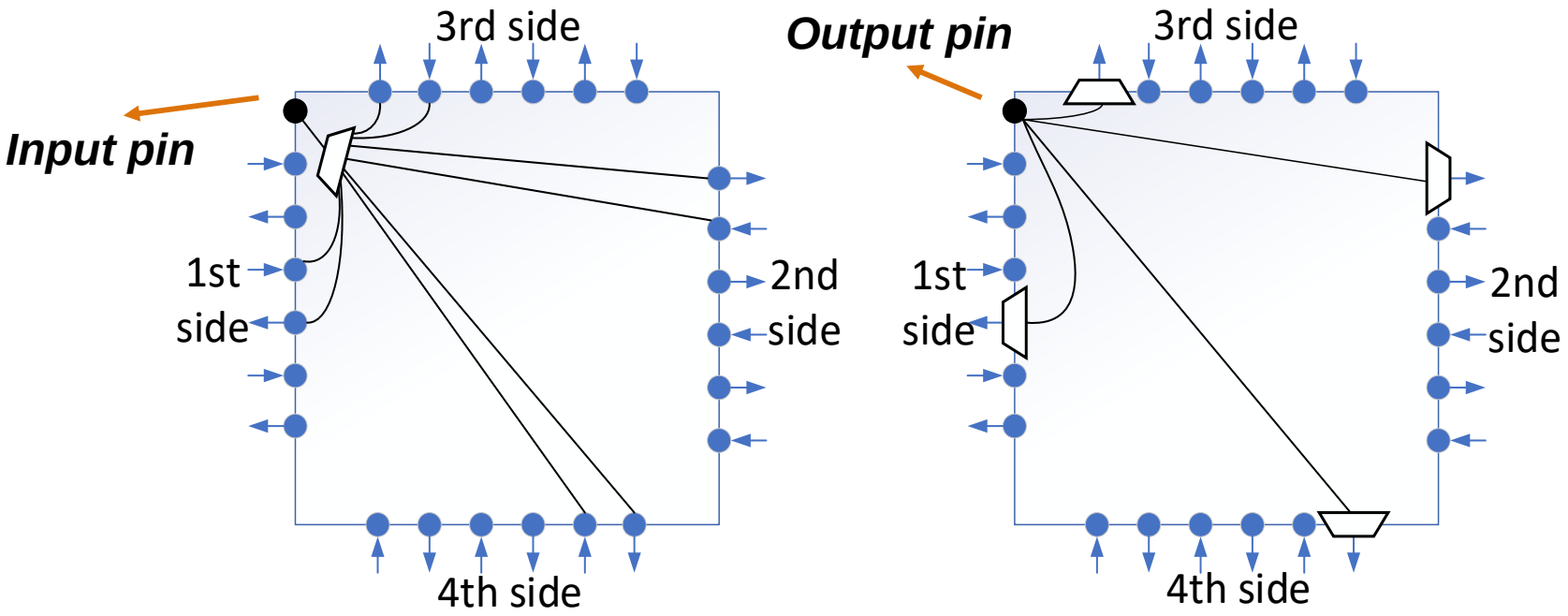
```
<!-- fc value is divided into four parts, which correspond to
four different GIB sides respectively -->

<fc in_type="frac" in_val="fc_in1 fc_in2 fc_in3 fc_in4"
out_type="frac" out_val="fc_out1 fc_out2 fc_out3 fc_out4"/>


<!--fn value defines the connections between output pins and
input pins through neighbor interconnect -->

<neighbor_interconnect fn=3 />
```

Fig.12 Enhanced XML tags for *fc* and *fn* values



GIB architecture

- $fc,in = (0.33\ 0.33\ 0.33\ 0.33)$
- $fc,out = (0.33\ 0.33\ 0.33\ 0.33)$



(a) Connections for input pins

(b) Connections for output pins

Fig.13 An example of LB pins connections in GIB

GIB architecture

- *fn* = 3
- Radius [10]: the distance of two LBs that connect with each other through neighbor interconnects

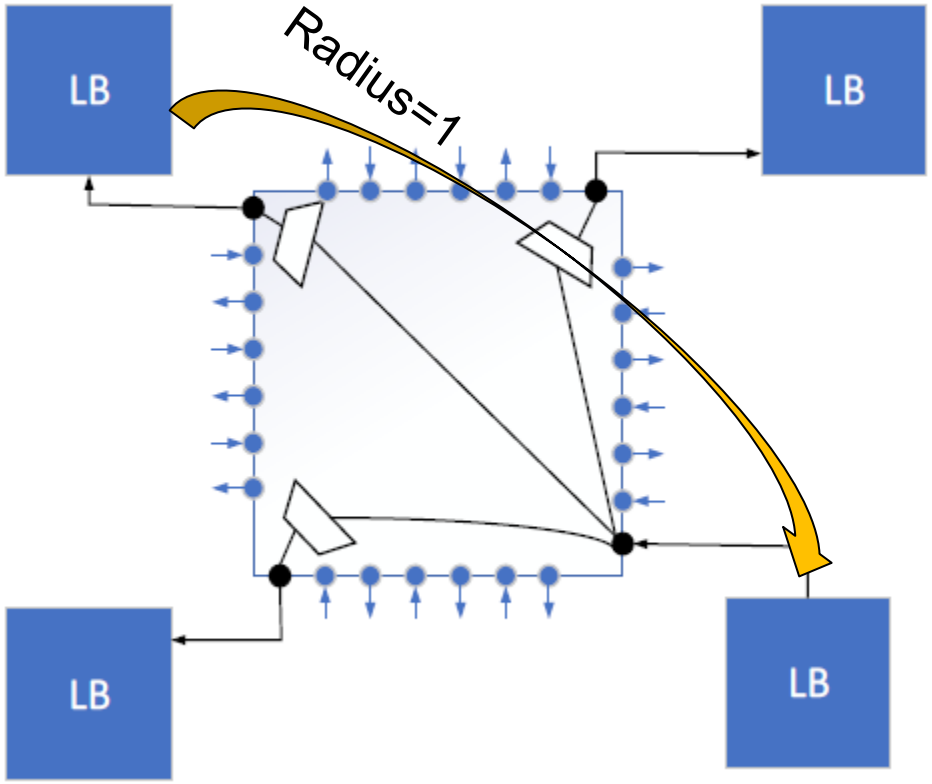


Fig.14 Neighbor interconnects in GIB architecture

[10] A. Roopchansingh and J. Rose, “Nearest neighbour interconnect architecture in deep submicron FPGAs,” IEEE Custom Integrated Circuits Conference, 2002, pp. 59–62.

GIB architecture

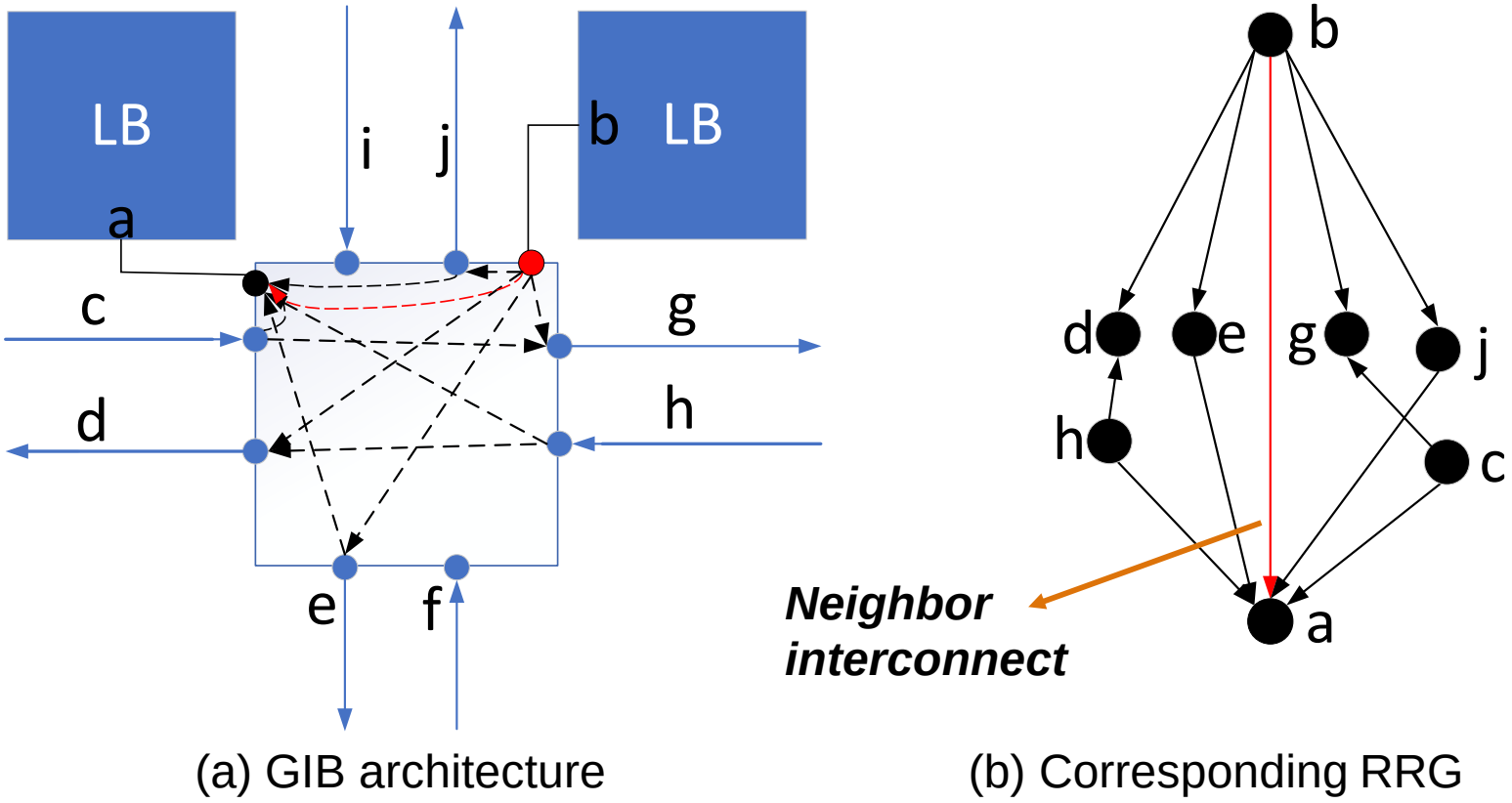
Table I. Percentage of net connections with radius = 1

(Δx, Δy)	Percentage
(1, 0)	8.9%
(0, 1)	10.5%
(1, 1)	9.3%
Sum	**28.7%**

Table II. Percentage of inter-cluster delay with radius = 1 on the critical path

(Δx, Δy)	Percentage
(1, 0)	2.8%
(0, 1)	4.2%
(1, 1)	4.4%
Sum	**11.4%**

GIB architecture



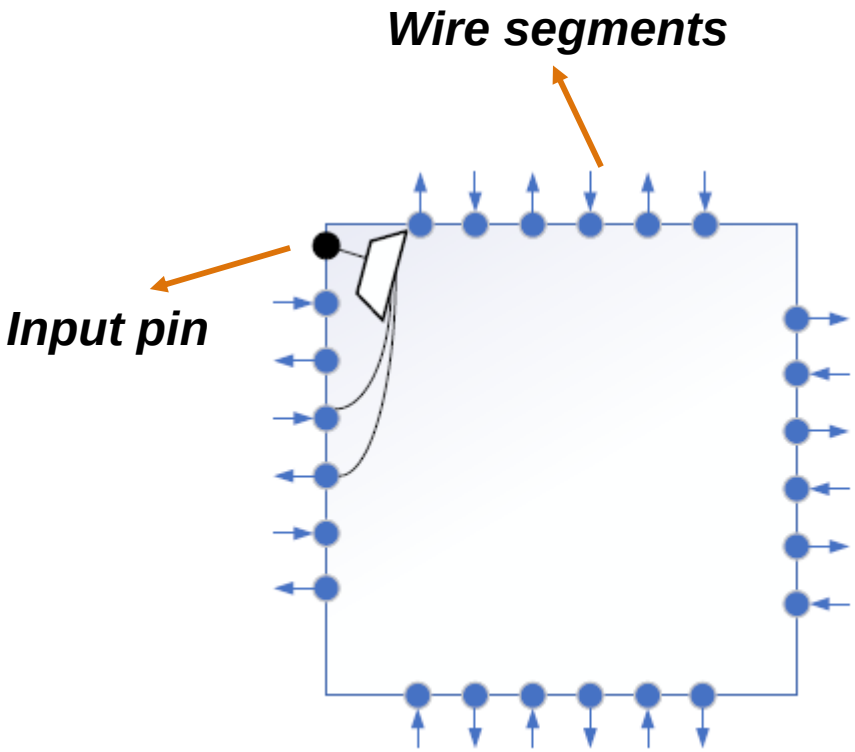
(a) GIB architecture

(b) Corresponding RRG

Fig.15 Routing Resource Graph(RRG)

GIB architecture

GIB architecture can also be simplified as CB-SB architecture.



- $fc = (fc1\ 0\ 0\ 0)$
- $fn = 0$

Fig.16 CB-SB modelling in GIB

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Experimental result

Table III. Baseline architecture parameters

LB	ten 6-input fracturable LUTs
LB input crossbar	50% populated
DSP	36×36 fracturable multipliers
Memories	configurable 32K block RAMs
SB	Wilton
L	4
W	300
fc,in	0.1
fc,out	0.1
fs	3

Experimental result

Table IV. Result of GIB with symmetry *fc* values compared with CB-SB architecture

fc	Area Ratio	Critical Path Delay Ratio	Area-Delay Ratio
0.1	98.2%	90.5%	88.9%
0.12	98.1%	92.7%	91.0%
0.16	98.0%	92.9%	91.0%
0.2	98.4%	90.8%	89.4%
Avg. improvement	**1.8%**	**8.3%**	**9.9%**

- CB-SB architecture
  - ✓ $fc,in = 0.1$
  - ✓ $fc,out = 0.1$
- GIB architecture
  - ✓ $fc,in = (0.025\ 0.025\ 0.025\ 0.025)$
  - ✓ $fc,out = (0.05\ 0.05\ 0.05\ 0.05)$

Experimental result

- The IOs or LB pins in the perimeter of FPGA device can't connect to all four sides of GIBs.

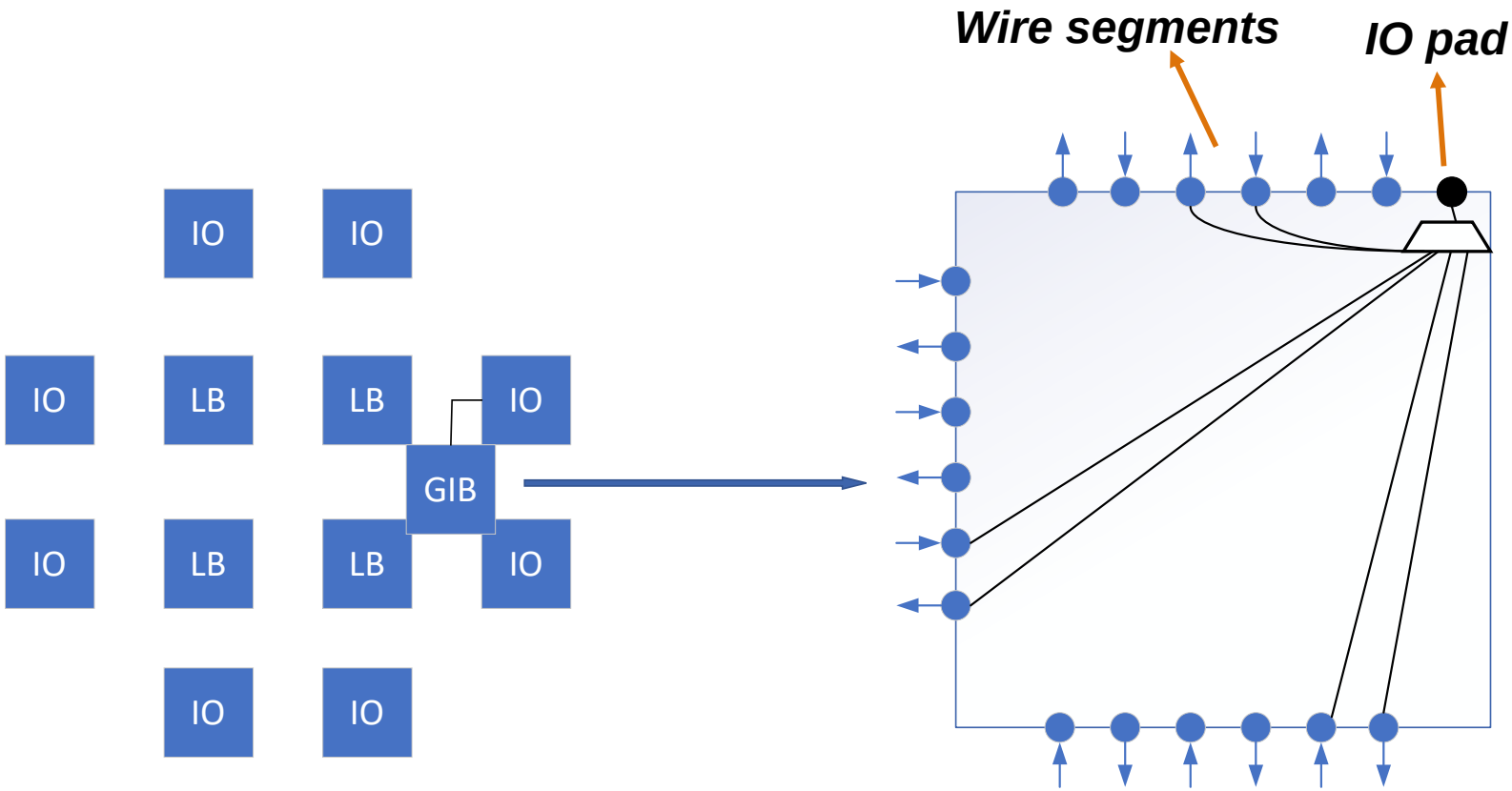
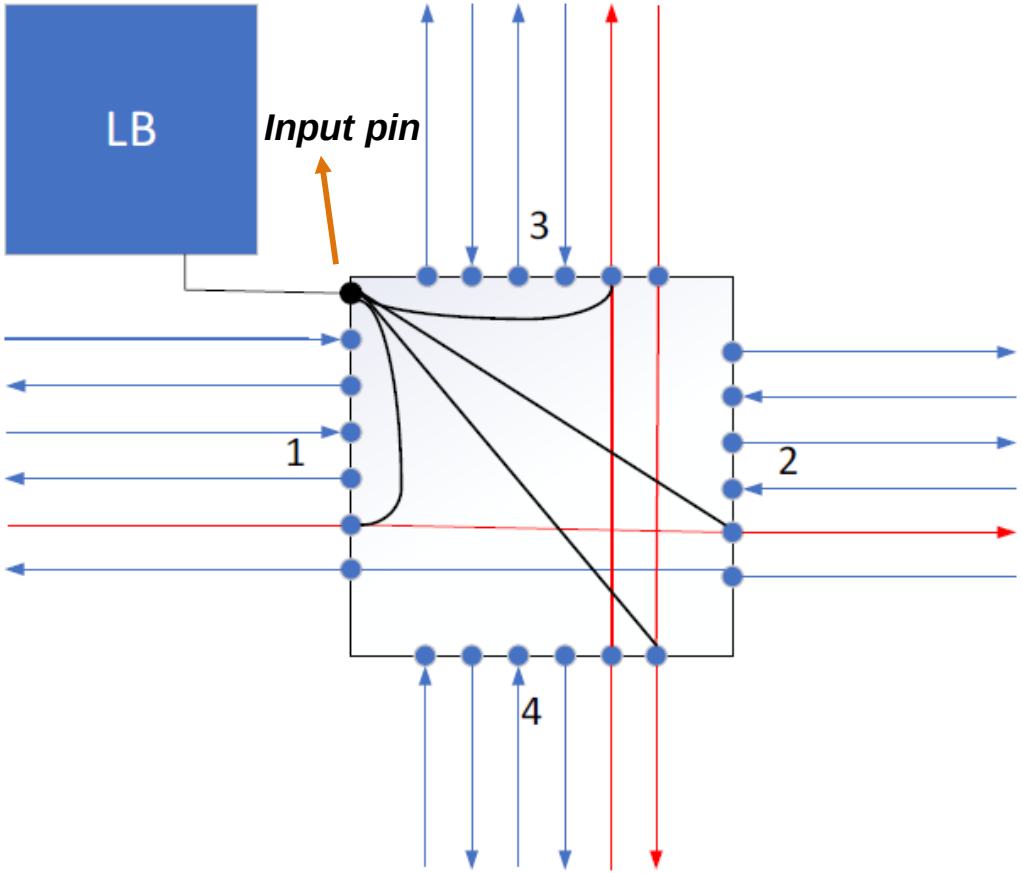


Fig.17 An example of IO connects to GIB

Experimental result

- An input pin may connect to a wire segment repeatedly.



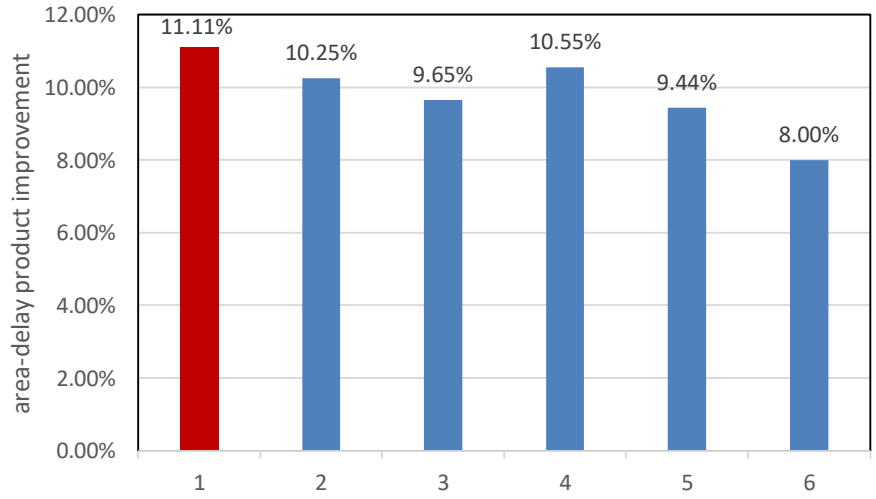
- $fc = (0.17\ 0.17\ 0\ .17\ 0.17)$
- $W = 6$

Fig.18 Connections between input pin and wire segments

Experimental result

Table IV. Groups of GIB architecture with different *fc* distributions

Group	*fc, in*	*fc, out*
1	**(0.025 0.025 0.025 0.025)**	**(0.05 0.05 0.05 0.05)**
2	(0.04 0.01 0.04 0.01)	(0.05 0.05 0.05 0.05)
3	(0.03 0.02 0.025 0.025)	(0.08 0.08 0.02 0.02)
4	(0.025 0.025 0.025 0.025)	(0.07 0.07 0.03 0.03)
5	(0.03 0.02 0.025 0.025)	(0.05 0.05 0.05 0.05)
6	(0.03 0.02 0.03 0.02)	(0.05 0.05 0.05 0.05)



Experimental result

Table IV. Comparison of GIB and CB-SB baseline architecture

fc, in	*fc, out*	Area Ratio	Critical Path Delay Ratio	Area-Delay Ratio
(0.03 0.03 0.03 0.03)	(0.05 0.05 0.05 0.05)	99.3%	92.7%	92.1%
(0.025 0.025 0.025 0.025)	(0.04 0.04 0.04 0.04)	97.0%	92.6%	89.8%
(0.025 0.025 0.025 0.025)	(0.05 0.05 0.05 0.05)	**98.2%**	**90.5%**	**88.9%**
(0.025 0.025 0.025 0.025)	(0.06 0.06 0.06 0.06)	99.4%	91.5%	90.9%
(0.03 0.03 0.03 0.03)	(0.06 0.06 0.06 0.06)	100.5%	92.4%	92.8%
(0.04 0.04 0.04 0.04)	(0.05 0.05 0.05 0.05)	101.7%	89.8%	91.3%
(0.04 0.04 0.04 0.04)	(0.08 0.08 0.08 0.08)	105.3%	91.7%	96.6%
(0.05 0.05 0.05 0.05)	(0.10 0.10 0.10 0.10)	110.9%	90.6%	100.5%

	Area	Critical Path Delay	Area-Delay
Avg. improvement	1.8%	9.5%	11.1%

Experimental result

Table V. Result of GIB compared with CB-SB architecture with wire segments of different lengths

Length	Area Improvement	Critical Path Delay Improvement	Area-Delay Improvement
2	0.7%	3.3%	4.0%
3	2.4%	6.6%	8.8%
4	1.8%	9.5%	11.1%
6	**1.0%**	**12.6%**	**13.5%**

- longer wire segments → more improvement.
- GIB architecture with length-6 wire segments improve the area-delay product by 13.5%.

Experimental result

- Length-4 wires
- *fs* = 3

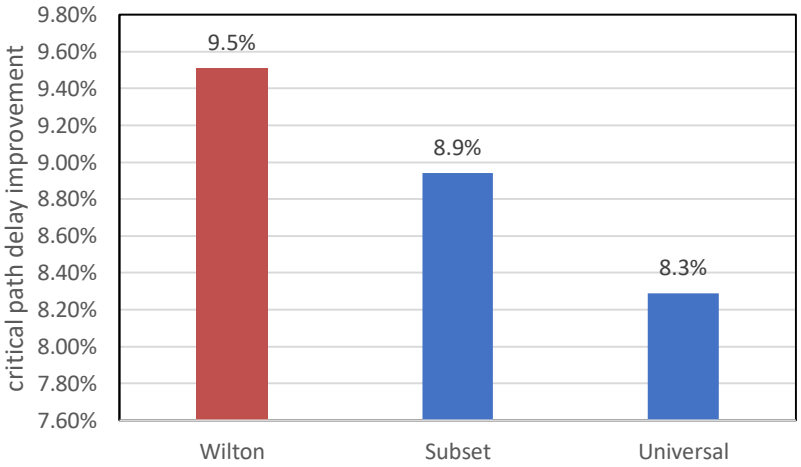


Fig.19 The area-delay product improvement in GIB with different SB patterns

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Conclusion & Future work

Conclusion

- A novel unidirectional interconnection architecture, GIB is proposed and evaluated in VTR 8.
- GIB architecture can improve the critical path delay by 9.5% and achieve area-delay product savings by 11.1% on average.

Future work

- Explore different wire segments and bent wire pattern to improve the GIB architecture further.
- Explore the placement and routing algorithms in VTR to improve the performance of GIB architecture.

THANK YOU